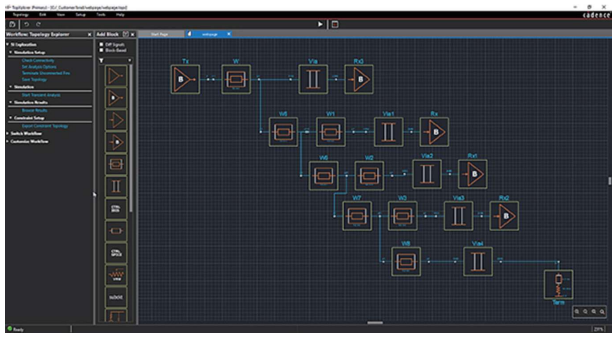
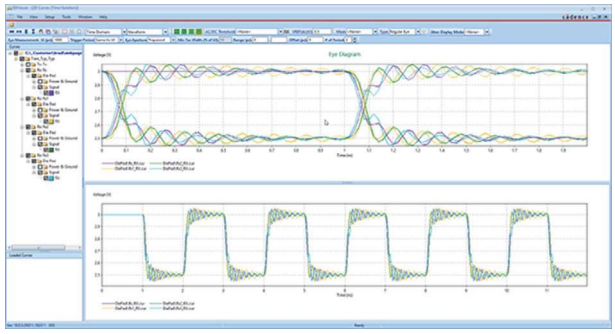
Pre / Post SI Simulation Solutions

Cadence Sigrity Topology Explorer

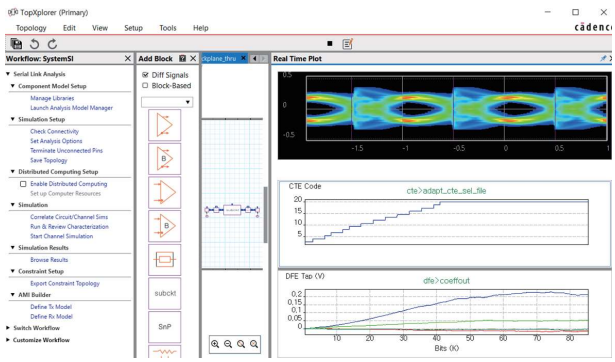
Cadence Sigrity Topology Explorer는 Signal, Power 그리고 이 모두를 고려한 What-if analysis가 가능한 범용 Topology Exploration Tool로서 Interconnect Model을 활용하여 Single Board 뿐만 아니라 System Board에 대한 SI/PI 해석환경을 제공합니다.



< Topology configuration with variety blocks like S parameter, SPICE circuit, IBIS, Via, etc. >



< Signal quality verification by time domain simulation results like eye diagram >



< Serial Link Simulation using IBIS-AMI >

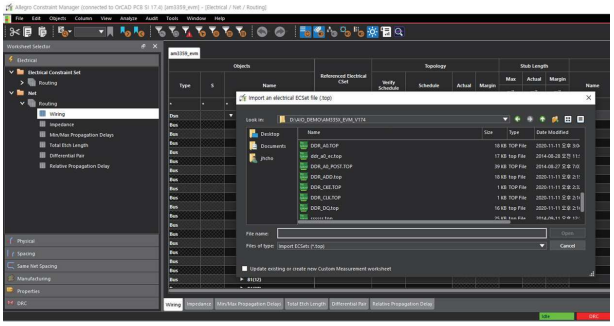
Features

- A general-purpose topology exploration environment for what-if analysis of signals, power, or both signals and power together
- Enables SI/PI analysis using interconnect models that are pre-route, captured from measurement, or extracted using EM tools
- Utilizes the same user interface as Sigrity SystemSI software, but will work on any signal, group of signals, or interface

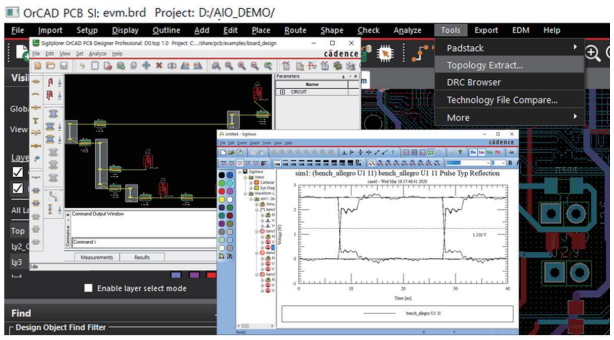
OrCAD PCB SI

OrCAD PCB SI는 Signal Integrity Issue를 회로설계단계에서부터 부품배치, Routing을 통한 PCB설계에 이르기까지 통합적으로 분석할 수 있는 환경을 제공합니다.
이와 같은 Pre Route 및 Post Route Topology Exploration을 통해 최상의 Interconnect 구성을 확인하고 신호해석 및 검증과 함께 Design Flow에 의한 완벽한 PCB 설계를 통해 개발기간을 단축할 수 있습니다.

< Pre- route signal analysis at circuit design stage for PCB design rule >



< Import the design rule by pre- route analysis result with topology >



< Post route SI analysis and verification >

Features

- Pre- and post-layout capabilities enable signal integrity exploration and analysis at any stage of the design cycle
- Exploration, analysis, and design of interconnect topologies help increase circuit reliability, improve circuit performance, and reduce prototypes and re-spins
- Direct integration with OrCAD PCB Editor and OrCAD Capture eliminates the need to translate design databases for simulation
- Analysis results can be converted into embedded constraints to drive known-good interconnect requirements throughout the design flow
- Support for all the latest industry-standard IBIS formats and models, generic models, and custom built models speeds time to simulation
- Proven, scalable, signal integrity exploration and validation solution that grows as design challenges and requirements evolve

VTK
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